Remarks

Applicants thank the examiner for the careful examination of this application and the clear explanation of the rejections.

Claims 1-19 and 27-34 are canceled.

Independent claim 20 defines an electronic system comprising a functional circuit and a selector circuit.

The functional circuit has a mode input lead receiving a mode signal to place the functional circuit in one of a functional mode in which the functional circuit operates normally and a test mode in which at least part of the functional circuit is disabled.

The selector circuit has a mode output lead connected to the mode input lead of the functional circuit and has a pair of clock leads separate from the functional circuit. Only one of the clock leads at one time receives a clock signal that controls the state of the mode signal formed on the mode output lead.

In contrast, US 5,347,523 to Khatri, et al., discloses a serial scan chain 16 that can send and receive data in parallel, through write and read circuits 80 and 83, to and from such as microprocessor circuits (not shown). The serial scan chain 16 provides for the concurrent output of an output serial stream of data via conductor 36. The conductor 36 is connected to an enable circuit 21, which is usually a tri-state buffer or multiplexer. The enable circuit 21 provides a selected output signal via a conductor 26 in response to an address match signal provided by conductor 28.

The details of the functional circuit and selector circuit of claim 20 distinguish over the serial scan chain 16, data conductor 36, and enable circuit 21 of the Khatri patent.

The Khatri patent further does not teach or suggest the limitations of the depending claims.

Claim 21 requires the test mode to be a by-pass mode.

Claim 22 requires the selector circuit to include state machine circuits coupled to the pair of clock leads.

Claim 23 requires the pair of clock leads to be both capable of receiving and sending clock signals.

Claim 24 requires the selector circuit to include a state machine circuit, and requires each of the clock leads to be coupled to the state machine circuit through a clock input buffer and be connected to the other clock lead through a clock output buffer.

Claim 25 requires the selector circuit to include another pair of clock leads separate from the functional circuit and requires at least one of the four clock leads to receive a clock signal that controls the mode signal.

Claim 26 requires the selector circuit to include another pair of clock leads separate from the functional circuit, and requires each of the another pair of clock leads to be coupled to

the state machine circuit through a clock input buffer and be connected to the other clock lead through a clock output buffer.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination.

Respectfully submitted,

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